NAGARJUNA COLLEGE OF ENGINEERING AND TECHNOLOGY	**NAGARJUNA COLLEGE OF ENGINEERING AND TECHNOLOGY** NAAC Accredited with "A+" grade Autonomous Institute under Visvesvaraya Technological University (VTU) **DEPARTMENT OF Electronics & Communication Engineering**

COURSE PLAN

(To be submitted before commencement of semester)

Course Name: Microcontroller & ARM Microprocessor	**Course Code:** 21ECI52	
Course Credits: 3:0:1:0	**Course L:T:P:** 3:0:1:0	**Semester: 5**
Course Teacher/s: Mr. Sunil Kumar B S(CC) Mrs. Bugide Sree Vidya	**Academic Year:** 2023-24	
Lab. Instructors (if applicable): Mr. Harish M C	**Date of Commencement of Class:**	

COURSE DESCRIPTION:

Student will earn the basic organization of a computing system by having glimpse of 8 bit and 16-bit processor architectures. During lab students gain hands on experience of 16-bit microprocessors to implement that on the ARM controllers.

They also gain the knowledge of the memory systems and architecture of the 8086 processors. They will gain profound knowledge of instruction sets of x86, in assemble language programming.

The architectural characteristics as well as instruction sets of 32-bit ARM Cortex M3 is also learnt by the students. The basic knowledge of the ARM Cortex M3 programming is also learnt in this course.

PREREQUISITES (if Any):

Concepts of Logic Design, number system.

LECTURE PLAN:

Topic	Topic Details	Lecture No.	Week	Unit/Chapter Text Book / Reference Books	Percentage of Syllabus coverage
Module-I	Basic Operational Concepts, Bus Structures	1	Week-1	Chapter:1/ T1 Page No: 7-10	**20%**
	Performance Processor Clock	2	Week-1	Chapter:1/ T1 Page No: 11-12	
	Basic Performance Equation, Clock Rate	3	Week-1	Chapter:1 / T1 Page No: 14-16	
	Performance Measurement	4	Week-2	Chapter:1 / T1 Page No: 17-19	
	Introduction to Microprocessor: Microprocessor architecture	5	Week-2	Chapter1-3/ T3 Page No: 3-59	
	and its operations, Memory	6	Week-2	Chapter:3/ T3 Page No: 63-80	
	Input & output devices, The	7	Week-3	Chapter:3/ T3 Page No: 80-81	

	8085				
	MPU- architecture, Pins and signals, Timing Diagrams	8	Week-3	Chapter1-4/ T3 Page No: 109-116	
	Cumulative Coverage				**20%**
Module II	Memory System: Basic Concepts, Semiconductor RAM Memories	9	Week-4	Chapter 4/ T3 Page No: 116-123	**20%**
	Read Only Memories, Speed, Size, and Cost,	10	Week-4	Chapter:2 / T1 Page No:36-42	
	Cache Memories – Mapping Functions	11	Week-4	Chapter:2 / T1 Page No:36-42	
	Replacement Algorithms, Performance Considerations. Introduction to 8086	12	Week-5	Chapter: 1/ T4 Page No:1.10-1.13	
	Microprocessor Evolution and types, 8086 Internal	13	Week-5	Chapter: 1/ T4 Page No:1.10-1.13	
	Architecture: The BIU and the Execution Unit	14	Week-5	Chapter: 2/ T4 Page No: 2.10-2.14	
	Segmentation, Pin Diagram of 8086, Introduction to Programming the 8086.	15	Week-6	Chapter: 2/ T4 Page No:2.10-2.14	
	Cumulative Coverage				**40%**
AAT 1	Quiz		Week-6		
Module III	Addressing Modes of 8086, Assembler Directives	16	Week-6	Chapter: 3,6/ T4 Page No: 3.23-3.27 6.29-6.33	**20%**
	Instruction Set of 8086. Data Transfer Instructions	17	Week-6	Chapter: 2,3/ T4 Page No:2.4-2.7 3.6-3.8	
	Arithmetic Instructions, Bit Manipulation Instructions	18	Week-7	Chapter: 2/ T4 Page No: 2.4-2.7	
	Branching Instructions,	19	Week-7	Chapter:3/ T4 Page No: 3.8-3.10	
	Processor Control Instructions	20	Week-7	Chapter:4/ T4 Page No:4.2-4.4	
	String Instructions.	21	Week-8	Chapter:5/ T4 Page No:5.1-5.37	
	8086 Assembly Language	22	Week-8	Chapter: 3/ T4 Page No: 3.23-3.27	
	Macros, Procedures, Assembly Language Programming Examples	23	Week-8	Chapter:5/ T4 Page No:5.1-5.37	

	Cumulative Coverage				**60%**
Module IV	Introduction, RISC design philosophy	24	Week-9	Chapter:1/ T2 Page No:4-6	**20%**
	ARM design philosophy, Embedded system hardware – AMBA bus protocol	25	Week-9	Chapter:1/ T2 Page No:6-9	
	ARM bus technology, Memory, Peripherals	26	Week-9	Chapter:1/ T2 Page No:9-12	
	Embedded system software – Initialization (BOOT) code, Operating System	27	Week-10	Chapter:1/ T2 Page No:13-14	
	Applications. ARM Processor Fundamentals	28	Week-10	Chapter:1/ T2 Page No:12-16	
	ARM core dataflow model, registers	29	Week-10	Chapter:2/ T2 Page No:22-29	
	current program status register Pipeline	30	Week-10	Chapter:2/ T2 Page No:22-29	
	Exceptions, Interrupts and Vector Table, Core extensions.	31	Week-11	Chapter:2/ T2 Page No:29-33	
	Cumulative Coverage				**80%**
AAT2	Surprise Test	32	Week-11	Chapter/ T Page No:	
	Introduction to the ARM Instruction set: Introduction,	33	Week-11	Chapter:3/ T2 Page No:47-84	
	Data processing instructions,	34	Week-12	Chapter:3/ T2 Page No:47-84	
	Load - Store instruction, Software	35	Week-12	Chapter:3/ T2 Page No:47-84	
	Interrupt instructions	36	Week-12	Chapter:3/ T2 Page No:47-84	
	Program status register instructions	37	Week-12	Chapter:3/ T2 Page No:47-84	
	Loading constants	38	Week-13	Chapter:3/ T2 Page No:47-84	
Module V	ARMv5E extensions	39	Week-13	Chapter:3/ T2 Page No:47-84	**20%**
	Conditional Execution.	40	Week-13	Chapter:3/ T2 Page No:47-84	
	Cumulative Coverage				**100%**

TEXTBOOKS AND REFERENCE BOOKS:

Book Type	Code	Title & Author	Publication Information		
			Edition	Publisher	Year
Text Books	T1	Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization. (Listed topics only from Chapters 1, 2, 4, 5, 8).	5th Edition	Tata McGraw Hill	2002
	T2	Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide"	1st Edition,	Elsevier, Morgan Kaufman publisher	2008
	T3	Ramesh Gaonkar, "Microprocessor Architecture, Programming, and Applications with the 8085"	6th Edition	Penram International Publication (India) Pvt. Ltd	2013
	T4	Douglas V. Hall, "Microprocessors and Interfacing: Programming and Hardware"	Revised 2nd Edition	TMH	2006

COURSE OUTCOMES:

At the end of the course the student will be able to:

CO1	Explain the basic organization of a computer system and the architecture of the 8085 microprocessors.
CO2	Demonstrate the functioning of memory systems and architectural, basics concepts of 8086.
CO3	Explicate the concepts of instruction sets in 8086 Assembly language programming.
CO4	Discuss the architectural characteristics as well as the instructions of the 32-bit microprocessor ARM Cortex M3.
CO5	Understand the ARM Cortex M3 programming instructions.

CO-PO MAPPING:

POS / COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C2.1	3	2	3	-	-	-	-	-	-	-	1	-
C2.2	3	2	3	-	-	-	-	-	-	-	1	-
C2.3	3	3	2	-	2	-	-	-	-	-	1	-
C2.4	2	2	2	-	-	-	-	-	-	-	1	-
C2.5	3	3	2	1	2	-	-	-	-	-	1	-

COURSE EVALUATION SCHEME:

Component		Weightage (%)		
CIE's	CIE 1 5th week	20	60	Average of 3 tests for20 marks
	CIE 2 10th week	20		
	CIE 3 15th week	20		
AAT's	AAT-1 10th week			10
	Lab Test	30		Reduced to 10
	Lab Record	20		10
Continuous Internal Evaluation Total Marks :100. Reduced to 50 Marks				
Semester End Examination (SEE) Total Marks :100. Reduced to 50 Marks				

Signature of the Course Co-Ordinator **Signature of the HOD**

Date: