NAGARJUNA COLLEGE OF ENGINEERING AND TECHNOLOGY
NAAC Accredited with "A" grade(An ISO 9001 – 2008
Certified Institution)
Affiliated to Visvesvaraya Technological University (VTU)
Recognized by Govt. of Karnataka & Approved by A.I.C.T.E. New Delhi
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course Handout

General Handout for all courses appended to the time table

Course No. : 22ECI32	**Dept.: Electronics and Communication Engineering**
Course Title : Analysis and Design of Digital Circuits	**Semester: IIIrd**
Instructor-in-charge : **Sreenivasulu K N** sreeni1005@ncetmail.com **Jyothi S K** jyothisk53@ncetmail.com	**Academic Year: 2023-24**
Lab. Instructor : Mr. Harish M C	**Date**: 16-11-2023

Subject Description:

This Course covers the fundamentals of switching theory to the solution of logic design problems. This means that the students will learn both the basic theory of switching circuits and how to apply it. After a brief introduction, the students will study Boolean algebra, which is the basic mathematical tool needed to analyze and synthesize an important class of switching circuits. Starting from a problem statement, the students will learn to design circuits of logicgates that have a specified relationship between signals at the input and output terminals. Then the students will study the logical properties of flip-flops, which serve as memory devices in sequential switching circuits. By combining flip-flops with circuits of logic gates, the students will learn to design counters, adders, sequence detectors, and similar circuits. The purpose of thiscourse is to develop the strong fundamentals in Logic Design and to apply switching theory tothe solution of logic design problems.

Text Books:

T1. John M Yarbrough: "Digital Logic Applications and Design", 3rd Edition, Cengage Learning, New Delhi, Reprint, 2012, ISBN-13: 978-81-315-0058-3, ISBN-10: 81315-0058-6.

T2. Donald D Givone: "Digital Principles and Design", 1st Edition, Tata McGraw Hill, New Delhi, Reprint, 2005, ISBN: 0-07-052906-X.

REFERENCE BOOKS:

R1. Charles H Roth: "Fundamentals of logic design", 5th Edition, Thomson, New Delhi, Reprint, 2007, ISBN: 81-315-0043-8.

R2. M. Morris Mano and Charles R. Kime: "Logic and computer design Fundamen- tals", 2nd Edition, Pearson, Reprint, 2005, ISBN: 81-7808-334-5.

CV, ME, ECE & ISE departments were accredited by NBA for 3 years

PREREQUISITES:

	Self-study	Remarks Students have completed this Courses.
1. Basic concepts of number system 2. Basic knowledge of electronic circuits		

LECTURE PLAN:

Topic	Topic Details	Number of Lectures	Unit/ Chapter Reference
Module – I **Principles of** **Combinational Logic**	Definition of combinational logic	1	T1 3.1
	Canonical forms	2	T1 3.2
	Generation of switching equations from truth tables	3	T1 3.3
	Karnaugh maps-three, four	4	T1 3.4.1
	Incompletely specified functions (Don't Care terms)	5	T1 3.4.2
	Simplifying Max term equations,	6	T1 3.5
	QuineMc-Clusky minimization technique	7	T1 3.6
	Map entered variable	8	T1 3.7
Module – II **Design and Analysis of** **combinational logic**	Parallel adder	9	T2 5.1
	Parallel subtractor	10	T2 5.1.1
	carry look ahead adder	11	T2 5.1.2
	Magnitude Comparator	12	T2 5.3
	Decoders	13	T2 5.4
	Encoders	14	T2 5.5
	Multiplexers	15	T2 5.6
	Logic Design with Multiplexers	16	T2 5.6.1
Revision			
AAT-1			

Module	Topic	No.	Reference
Module – III **Flip-Flops and its Applications**	The Master-Slave Flip-flops : SR flip-flops	17	T2 6.4.1
	JK flip flops.	18	T2 6.6, 6.7
	Characteristic equations, Registers Binary Ripple Counters	19	T2 6.8.1
	Counters based on Shift Registers	20	T2 6.8.3
	Synchronous Binary Counters,	21	T2 6.8.2
	Design of Synchronous mod-n Counter using clocked T,	22	T2 6.9.1
	Design of Synchronous mod-n Counter using clocked SR flip-flops	23	
	Design of Synchronous mod-n Counter using clocked JK flip-flops	24	
Module – IV **Sequential Circuits**	Characteristic Equations	25	T2 6.6
	Registers	26	T2 6.7
	Counters - Binary Ripple Counters	27	T2 6.8.1
	Synchronous Binary counters	28	T2 6.8.2
	Counters based on Shift Registers	29	T2 6.8.3
	Design of a Synchronous counters	30	T2 6.9
	Design of a Synchronous Mod-N Counter using clocked JK and D Flip-Flop	31	T2 6.9.1
	Design of a Synchronous Mod-N Counter using clocked T Flip-Flops	32	T2 6.9.2
Revision			
AAT-2			
Module – V **Sequential Design & Applications of Digital Circuits**	Introduction, Mealy and Moore Models	33	T1 8.1
	State Machine Notation	34	T1 8.2
	Present state, Next state, State diagram, State Table	35	T1 8.2.1
	Excitation table and Equations, Excitation Realization Cost	36	T1 8.2.2
	Synchronous Sequential Circuit Analysis	37	T1 8.3
	Analysis Principles and Examples	38	T1 8.4
	Construction of state diagram	39	T1 8.5
	Examples of construction of state diagram	40	T1 8.5.1

Course Outcomes

At the end of the course the student will be able to:

CO1	Simplify Boolean functions using K-map and Quine-McCluskey minimization technique.
CO2	Analyze and design for combinational logic circuits.
CO3	Apply the concepts of Flip Flops (SR, D, T and JK).
CO4	Design the Registers, Asynchronous and Synchronous counters.
CO5	Design the appropriate Mealy and Moore Finite State Machine.

CO-PO MAPPING:

POS COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
C202.1	2	3	2	1	-	-	-	-	-	-	-	2	2	2	1
C202.2	2	3	2	2	-	-	-	-	-	-	-	2	3	2	2
C202.3	1	2	3	1	-	-	-	-	-	-	-	1	2	3	3
C202.4	1	2	3	2	3	-	-	-	3	2	1	1	1	2	1
C202.5	1	2	3	2	3	-	-	-	3	2	1	1	2	1	1

Evaluation Scheme:

IPCC / Integrated Courses :						
Evaluation Type		**Component**	**Max Marks**	**Marks reduced to**	**Min. Marks**	**Evaluation Details**
Theory Component	Internal Assessment Tests(IAT)	IAT-1	25	15	10	Average of two IATs, Scaled down to 15 marks
		IAT-2	25			
	Comprehensive Continuous	CCE-1	10			Minimum of two Assessment methods as per 22OB4.2 of regulations ,

Component						Description
	Evaluations (CCE)			10		Average of two CCEs, scaled down to 10 marks
	CCE-2	10				
Total CIE - Theory			**25**	**10**		Scale down marks of IAT and CCE to 25
Laboratory Component	Practicals and Lab Records	-	15	**25**	**10**	Conduction of experiments and preparation of Lab records, etc
	Lab Test	50	10			One test to be conducted after the completion of all lab experiments.
Total CIE – Practicals			**25**	**10**		
Total CIE (Theory + Lab)			**50**	**20**		
SEE		100	**50**	**18**		Conducted for 100 marks and scaled down to 50.
CIE + SEE			**100**	**40**		

Notices: All notices will be displayed on NCET and in Department website.
Chamber Consultation Hour: Wednesday 2:00Pm to 4:00 Pm
Makeup Policy: To be granted only in case of serious illness or emergency.
Email Policy: Communication through email. If you want to discuss anything, you are most welcome to meet me during chamber consultation hours or immediately after the class.
Academic queries/doubts can be posted in Moodle.

Ms. Jyothi S K/Mr. Sreenivasulu K N   **Dr.Nagesh K N**
            HOD   **Course-in-charge**

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